Evaluation of Electronic Characteristics of Double Gate Graphene Nanoribbon Field Effect Transistor for Wide Range of Temperatures

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***Abstract*: In this paper the electronic characteristics of double gate graphene nanoribbon field effect transistor (GNRFET) at wide range of temperatures are evaluated. Temperature is varied from 250 to 450 ° K. The simulations are performed by the self-consistent solution of Poisson–Schrödinger equations, within the non-equilibrium Green's function (NEGF) formalism. A loop between these two equation is required. Different parameters of GNRFETs like saturation current, leakage current, sub-threshold swing, threshold voltage and current ration are evaluated in wide range of temperatures. Simulation results show that device threshold voltage decreases and sub-threshold swing increases at high temperatures. The results show that there is a linear relation between sub-threshold swing and temperature. Also, Saturation current is improved at high temperatures but at a same time the leakage current characteristic is damaged by applying higher temperatures. Decrease in leakage current is more noticeable than increase in saturation current thus the device current ratio decreases at high temperatures**.

***Keywords*: GNRFET, temperature variations, NEGF, subthreshold swing, current ratio, leakage current.**

1. INTRODUCTION

Nowadays, strong interest of researchers in graphene nanoribbons (GNRs) is due to their excellent electronic properties such as full planar processing, high carrier velocity for fast switching [2, 3]. There are some problems in carbon nanotubes (CNTs) which have been removed by GNRs. for example controlling the CNT chirality during the growth process is a big problem. Chirality (together with other factors) determines semiconductoring or metallic type of channel. From the experimental viewpoint the graphene material can be simply patterned using standard nanoelectronic lithography methods [4]. In spite of some of other low-dimensional nanostructures, GNRs with complicated sub-micrometer structures can now be fabricated by nanoelectronic fabrication methods. The opportunity of manufacturing devices with channels that are very slim will permit graphene field-effect transistors to be scaled to shorter channel lengths and higher speeds. Beside these valuable properties, at very short channels, the graphene field-effect transistors cannot be turned off effectively due to the high tunneling current, where their leakage current is high leading to an ON/OFF current ratio typically less than other FETs. This issue limits their application in logic circuits. We know that FETs current ratio is strongly affected by temperature. Temperature plays a key role in the field effect transistor performance and characteristics. Thus the performance of graphene nanoribbon field effect transistors should be predicted at different temperatures, too. Therefore, in this paper by varying temperature the characteristics of GNRFETs have been investigated using two-dimensional (2D) quantum simulation. The simulations have been done by the self-consistent solution of 2D Poisson Schrodinger formalism [4]. These investigations have been performed in terms of saturation current, off current, subthreshold swing, threshold voltage, and device current ratio. The rest of paper is organized as follows: section two includes simulation methods. Section three presents simulation results and discussions. Finally in last section we mention the conclusions.

2. DEVICE STRUCTURE AND SIMULATION METHOD

The simulated GNRFET structure includes two gates with two same oxides as gate insulator as shown in figure 1. Gate metals are the same and situated at up and down part of devices. An N=13 A-GNR is used in which N represents the number of dimmer carbon atoms. GNR is in the middle of structures and the devices have same symmetry. Channel is totally intrinsic while source and drain regions are doped by n-type doping. An N=13 A-GNR is used in which N represents the number of dimmer carbon atoms. GNR is in the middle of symmetric structure. Table 1 summarizes the devices physical parameters.

Table 1: GNRFET parameters used in simulation

Parameter	Value
GNR type	A-GNR
Source/Drain length	20 nm
Number of dimmer carbon atoms	13
Grid size in x direction	0.25 nm
Grid size in y direction	0.1 nm
Nearest neighbor hoping parameter	2.7 eV
Temperature	is varied
Gate dielectric constant	3.9
Dielectric thickness	2 nm
Source/Drain overlap with Gate	Without overlap
Channel length	20 nm

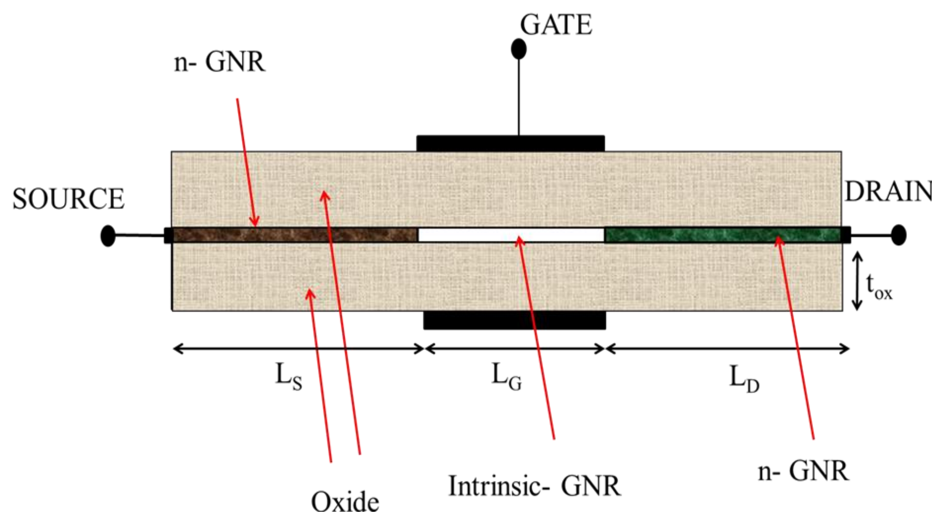

Figure 1.Schematic view of device structure of double gate GNRFET.

Poisson equation simulates potential distribution and transport equation simulates charge transport between source and drain regions. For simulating a double Gate GNRFETs behavior the transport (Schrodinger) and Poisson equations ought to be solved self-consistently. In this study, the performance of transistor is examined by solving the quantum transport equation based on the NEGF formalism [5, 6].The Poisson equation is [7]:

$$\nabla^2 U = \frac{-q}{\varepsilon}\rho \tag{1}$$

Where ρ is the net charge density distribution counting the doping density, U is the electrostatic potential, and ε is the dielectric constant.

The Poisson equation is solved numerically to estimate the self-consistent electrostaticpotential along the nanoribbon. The fresh potential distribution results in an adopted Hamiltonian. The output of transport equation is a new input for Poisson equation. After finishing the required loops the self-consistent loop between the electrostatic equation and the quantum transport is achieved.

By considering third nearest neighbor effects and edge bond relaxation and [5, 6], Hamiltonian matrix is given by following equation:

$$H = \begin{bmatrix} U_1 & b_{2q} & 0 & t_3 & & \\ b_{2q} & U_2 & b_{1q} & 0 & 0 & \\ 0 & b_{1q} & U_3 & b_{2q} & 0 & t_3 \\ t_3 & 0 & b_{2q} & U_4 & b_{1q} & 0 \\ & & 0 & b_{1q} & U_5 & \cdots \\ & & t_3 & 0 & \cdots & \cdots \end{bmatrix}_{N\times N} \quad (2)$$

Here, the diagonal element U_j corresponds to the on-site electrostatic potential along the tube.This value is estimated by solving the equation (1).t_3 describes the third nearest neighbor coupling in the transport direction. This value is $t_3=0.2eV$ in our simulations according to that in [5, 6].

After self consistent criteria is achieved, the current is obtained from Landaur–Buttiker formula [7, 8]:

$$I = \frac{2q}{h}\int T(E)[F(E-E_{FS}) - F(E-E_{FD})]dE \quad (3)$$

where$T(E)$ is the transmission coefficient and F is Fermi function. More details can be found in [9, 10, 11].

3. SIMULATION RESULTS

Current-voltage characteristics or output characteristics of GNRFET at room temperature (300 K) are illustrated in figure 2.

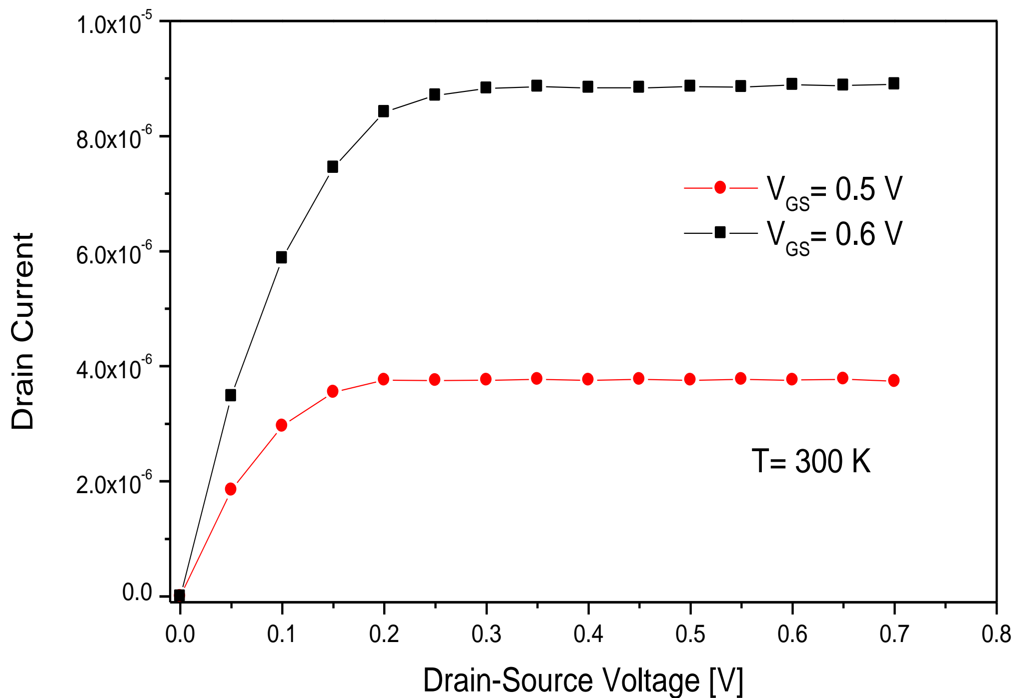

Figure 2. Output characteristics of GNRFET at room temperature (300 K).

These characteristics are reproduced for 450K at figure 3. The investigated voltages are 0.5 and 0.6 V for gate electrode at 0-0.7 V for drain electrode. It can be obviously seen that by increasing the temperature, the saturation current increases. For example, at gate voltage of 0.5 V and T=300K, the saturation current is less than 4 micro A, while for T=450K this value is more than 4.5 micro A.

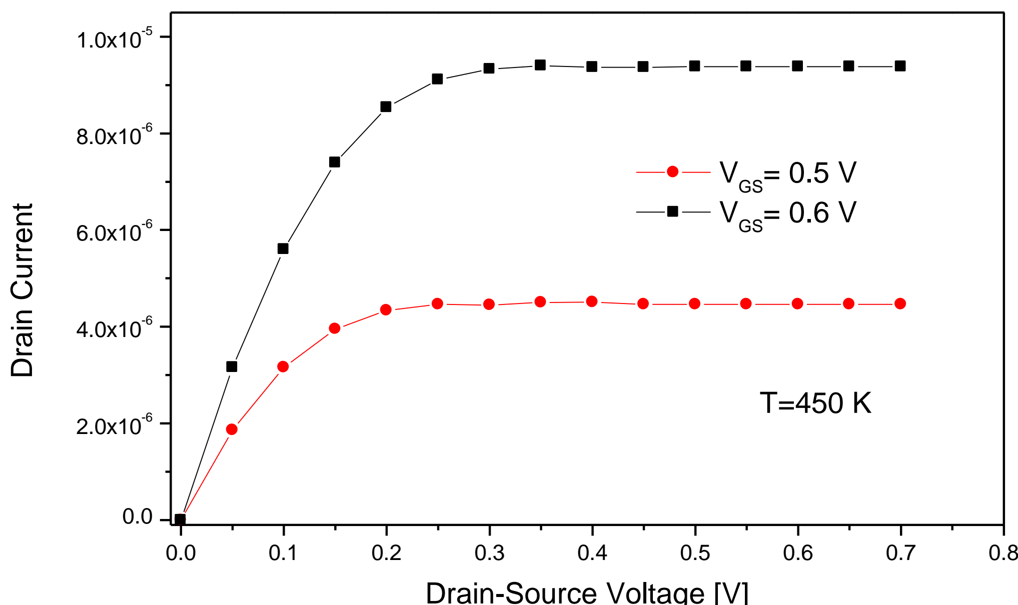

Figure 3. Output characteristics of GNRFET at room temperature (450 K).

Gate-source voltage versus drain source current at different drain source voltages are illustrated in figure 4 for 300K and in figure 5 for 400K. Increase in temperature increases the band to band tunneling (BTBT) and consequently damages the leakage current. The ambipolar behavior is apparent from figure 4. So, the device has better behavior at lower temperatures. Increase in leakage current is more noticeable than increase in saturation current so, the device current ratio decreases by increase in temperature.

The variations in off and saturation currents by temperature show that the device threshold voltage changes by temperature. Threshold voltage is one of the significant parameters of the nanoscale devices. Therefore, it is essential to investigate the effects of temperature on threshold voltage.Figure 6 shows the threshold voltage variationas a function of the temperature. Itcan be seen that by varying the temperature, the device showsan approximately large deviation which is undesirable for reliability of CMOS circuits. It can be observed that there is a linear inverse relation between threshold voltage and temperature. In other words, threshold voltage decreases by temperature linearly.

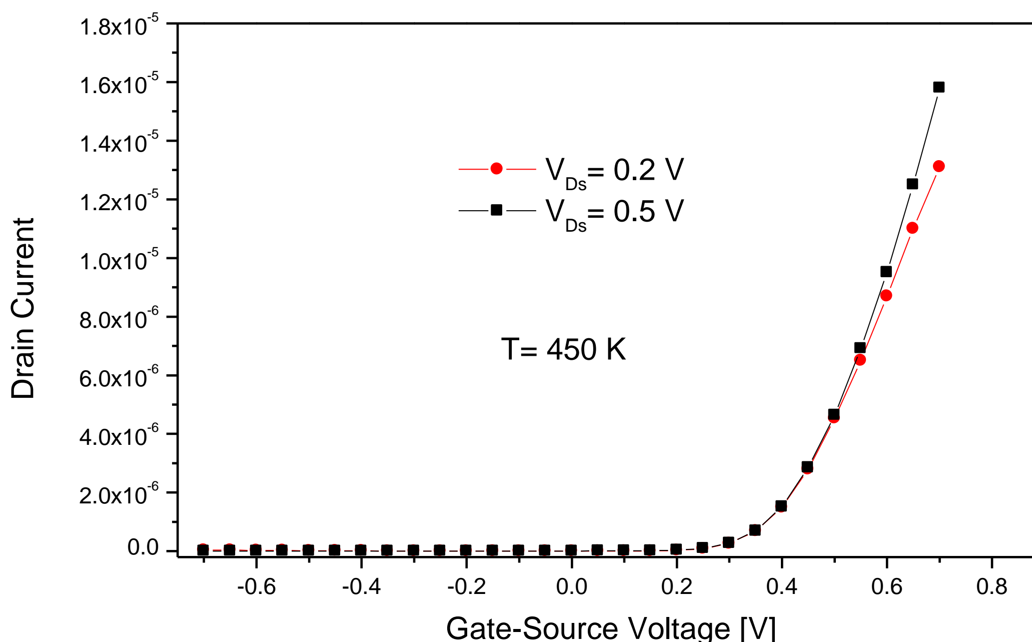

Figure 4.Gate-source voltage versus drain source current at different drain source voltages at T=300K

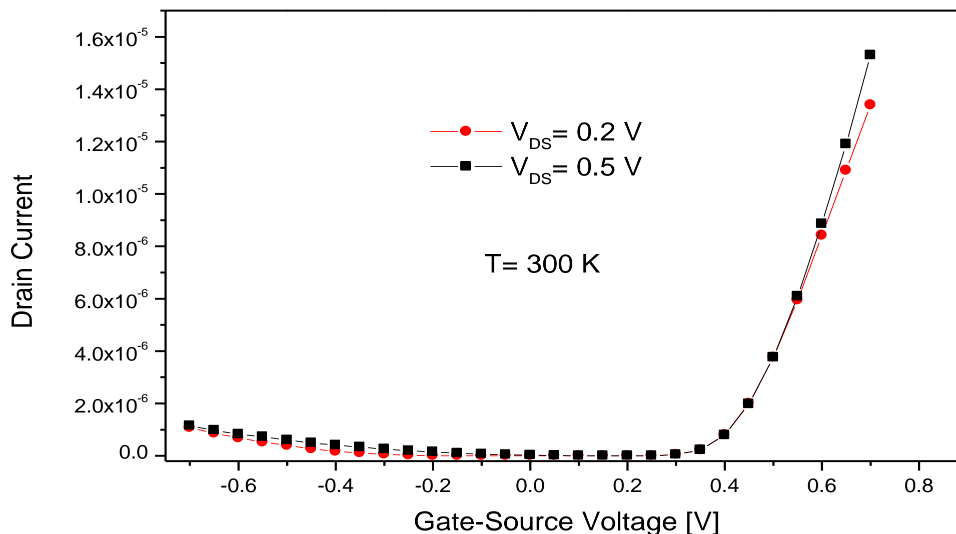

Figure 5. Gate-source voltage versus drain source current at different drain source voltages at T=450K.

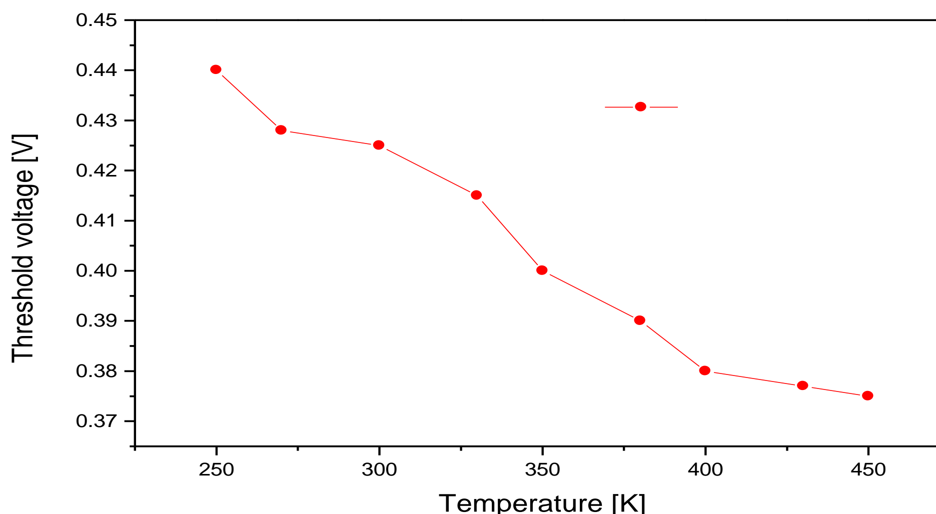

Figure 6. Threshold voltage variation by temperature from T=250K to 450K.

As the device channel shrinks, some effects called short channel effect (SCEs), damage the device performance. One of these effects is subthreshold swing (SS). The subthreshold swing is a key parameter in transistor miniaturization. Slighter subthreshold swing means greater subthreshold slope and consequently lower dissipation at subthreshold regime. A small subthreshold swing (S) is desired for low-power operation for field effect devices scaled down to tiny sizes [12]. Subthreshold swing is defined as ($S = \Delta V_{GS}/\Delta \log(I_{DS})$) atsubthreshold regime.

Sub-threshold swing versus temperature is illustrated in figure 7. It is obvious that the device experiences higher sub-threshold swings with increase in temperature. Here, the relation between SS and temperature is approximately linear, too. About two times increase in temperature from 250 to 450 results in more than two times increase in SS. This is a noticeable damage in short channel performance of small channel GNRFETs.

4. CONCLUSION

An NEGF formalism with an uncoupled mode space has been used in order to simulate the electronic properties of the GNRFETs with symmetric double gate structures at different temperatures. Temperature was raised from 250 to 450 K. Main device characteristics beside short channel parameters have been studied. The results show that the increase in temperature results in higher sub-threshold swing and lower current ratio. Also, the threshold voltage decreases by temperature. Saturation current improves but leakage current damages at high temperatures. The achievements of these study can be used for design considerations in GNRFET devices.

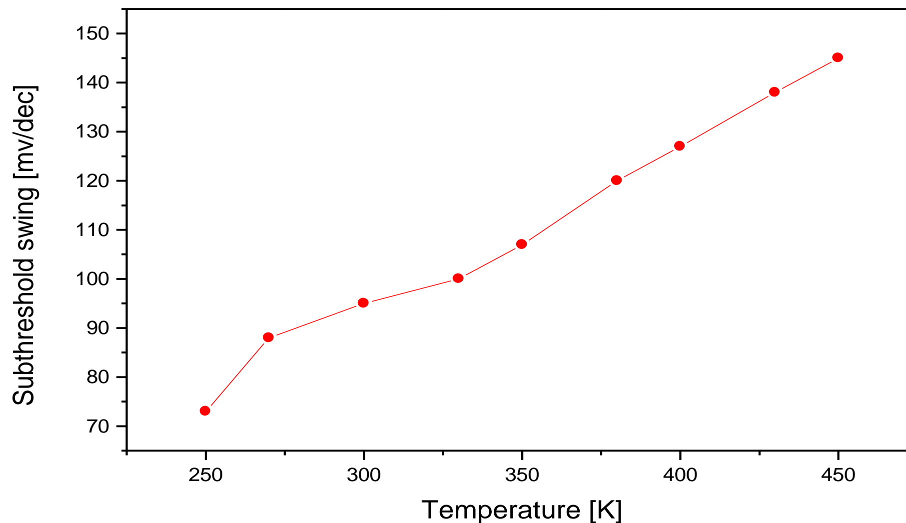

Figure 7.Subthreshold swing variation by temperature from T=250K to 450K.

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